

CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:
 - 2 a control signal source;
 - 3 a control signal destination;
 - 4 a control signal path having a length, the control signal path coupling the control signal
 - 5 source and control signal destination, comprising:
 - 6 a first plurality of signal paths each having two ends, a source end of a selected path
 - 7 of the first plurality of signal paths coupled to the control signal source;
 - 8 a second plurality of signal paths each having two ends, a destination end of a
 - 9 selected path of the second plurality of signal paths coupled to the control signal destination;
 - 10 a spanning circuit coupling the selected path of the first plurality of signal paths to
 - 11 the selected path of the second plurality of signal paths; and
 - 12 wherein the length of the control signal path is at least a the sum of a length of the selected
 - 13 path of the first plurality of signal paths and a length the selected path of the second plurality of
 - 14 signal paths.

- 1 2. The computer system as defined in claim 1 wherein the spanning circuit further comprises:
 - 2 a medial solder pad;
 - 3 a first zero ohm resistor connecting a remaining end of the selected path of the first
 - 4 plurality of signal paths to the medial solder pad; and
 - 5 a second zero ohm resistor connecting a remaining end of the selected path of the second
 - 6 plurality of signal paths to the medial solder pad.

1 3. The computer system as defined in claim 2 wherein the coupling between the control signal
2 source and the source end of selected path of the first plurality of signal paths further comprises:
3 a source solder pad coupled to said control signal source;
4 a zero ohm resistor connecting the source solder pad to the source end of the selected path
5 of the first plurality of signal paths.

1 4. The computer system as defined in claim 2 wherein the coupling between the control signal
2 destination and the selected path of the second plurality of signal paths further comprises:
3 a destination solder pad coupled to said control signal destination;
4 a zero ohm resistor connecting the destination solder pad to the destination end of the
5 selected path of the second plurality of signal paths.

1 5. The computer system as defined in claim 1 further comprising:
2 the control signal source is a clock source;
3 the control signal destination is a memory controller;
4 the control signal path is a clock signal path; and
5 wherein the memory controller uses a clock signal propagating on the clock signal path as a
6 read clock for reading data from a memory bus.

1 6. The computer system as defined in claim 1 further comprising:
2 the control signal source is a feedback output of a phased locked loop (PLL);
3 the control signal destination is a feedback input of the PLL; and

the control signal path is a feedback path of the PLL, and the length of the feedback path controls a phase relationship between an input signal to the PLL and an output signal of the PLL.

1 7. The computer system as defined in claim 1 wherein at least two of the first plurality of
2 signal paths have different lengths.

1 8. The computer system as defined in claim 7 wherein at least two of the second plurality of
2 signal paths have different lengths.

1 9. The computer system as defined in claim 1 wherein each of the first plurality of signal
2 paths have different lengths.

1 10. The computer system as defined in claim 9 wherein each of the second plurality of signal
2 paths have different lengths.

11. The computer system as defined in claim 10 wherein each of the first and second plurality
of signal paths have different lengths.

1 12. The computer system as defined in claim 11 wherein lengths of each of the signal paths in
2 the first and second plurality of signal paths are select so that each unique path through the control
3 signal path has a unique length.

1 13. A method of adjusting timing of a control signal from a signal source to a signal
2 destination, comprising:

3 coupling an adjustable signal path circuit having a plurality of possible signal path lengths
4 between the signal source and the signal destination;

5 adjusting a length of a signal path through the adjustable signal path circuit to selectively
6 add time delay to the control signal comprising:

7 selecting a first signal path in a first cluster of possible signal paths, said first signal
8 path having a length;

9 selecting a second signal path in a second cluster of possible signal paths, said
10 second signal path having a length;

11 coupling the first and second signal paths; and

12 forcing the control signal to propagate along the overall signal path having a length
13 comprising the first and second signal paths.

1 14. The method as defined in claim 13 wherein said selecting the first and second signal paths
2 further comprise:

3 coupling a source end of the first signal path to the control signal source using a zero ohm
4 resistor;

5 coupling a second end of the first signal path to a second end of the second signal path
6 using a zero ohm resistor; and

7 coupling a destination end of the second signal path to the control signal destination using a
8 zero ohm resistor.

1 15. The method as defined in claim 14 wherein coupling the second end of the first signal path
2 to a second end of the second signal path further comprises:

3 connecting the second end of the first signal path to a medial solder pad using a zero ohm
4 resistor; and

5 connecting the second end of the second signal path to the medial solder pad using a zero
6 ohm resistor.

1 16. The method as defined in claim 15 wherein coupling a source end of the first signal path to
2 the control signal source further comprises:

3 coupling the control signal source to a source contact pad; and

4 connecting the source end of the first signal path to the source contact pad by way of a zero

5 ohm resistor.

1 17. The method as defined in claim 15 wherein coupling a destination end of the second signal
2 path to the control signal destination further comprises:

3 coupling the control signal destination to a destination contact pad;

4 connecting the destination end of the second signal path to the destination pad by way of a

5 zero ohm resistor.

1 18. The method as defined in claim 13 further comprising:

2 selecting a unique length for each of the first cluster of possible signal paths;

3 selecting a unique length for each of the second cluster of possible signal paths; and

4 selecting said unique lengths for the first and second clusters of possible signal paths such
5 that each combination of the first and second signal paths have unique lengths.

1 19. A computer system comprising:
2 a control signal source;
3 a control signal destination;
4 a control signal path having a length, the control signal path coupling the control signal
5 source and control signal destination, comprising:
6 a first plurality of signal paths, a source end of a selected first path of the first
7 plurality of signal paths coupled to the control signal source;
8 a second plurality of signal paths, a destination end of a selected second path of the
9 second plurality of signal paths coupled to the control signal destination;
10 a third plurality of signal paths;
11 a first spanning circuit coupling the selected first path to a selected third path of the
12 of the third plurality of signal paths; and
13 a second spanning circuit coupling the selected third path to the selected second
14 path;
15 wherein the length of the control signal path is at least the sum of a length of the selected
16 first path, a length the selected second path, and a length of the selected third path.

1 20. The computer system as defined in claim 19 wherein the first spanning circuit further
2 comprises:
3 a first solder pad;

- 4 a first zero ohm resistor connecting the first solder pad to the selected first path; and
- 5 a second zero ohm resistor connecting the first solder pad to the selected third path.
- 1 21. The computer system as defined in claim 19 wherein the second spanning circuit further
2 comprises:
- 3 a first solder pad;
- 4 a first zero ohm resistor connecting the first solder pad to the selected third path; and
- 5 a second zero ohm resistor connecting the first solder pad to the selected second path.
- 1 22. The computer system as defined in claim 19 further comprising:
2 the control signal source is a clock source;
3 the control signal destination is a memory controller;
4 the control signal path is a clock signal path; and
5 wherein the memory controller uses a clock signal propagating on the clock signal path as a
6 read clock for reading data from a memory bus.
- 1 23. The computer system as defined in claim 19 further comprising:
2 the control signal source is a feedback output of a phased locked loop (PLL);
3 the control signal destination is a feedback input of the PLL; and
4 the control signal path is a feedback path of the PLL, and the length of the feedback path
5 controls a phase relationship between an input signal to the PLL and an output signal of the PLL.

1 24. The computer system as defined in claim 19 wherein only one source end of the first
2 plurality of signal paths couples to the control signal destination.

1 25. The computer system as defined in claim 19 wherein only one destination end of the
2 second plurality of signal paths couples to the control signal destination.

1 26. A computer system having a control signal between a first and second device, comprising:
2 a solder pad coupled to said first device;
3 a first signal path having a length;
4 a zero ohm resistor connecting said solder pad to said first signal path;
5 a second solder pad;
6 a second zero ohm resistor connecting said first signal path to said second solder pad;
7 a second signal path having a length;
8 a third zero ohm resistor connecting the second solder pad to said second signal path;
9 a third solder pad;
10 a fourth zero ohm resistor connecting the second signal path to the third solder pad;
11 where said third solder pad coupled to said second device;
12 a first plurality of unused signal paths spanning the first and second solder pads, but not
13 electrically connecting those pads; and
14 a second plurality of unused signal paths spanning the second and third solder pads, but not
15 electrically connecting those pads;
16 wherein said first device drives a control signal across said first and second signal paths,
17 and wherein said second device reads said control signal; and

18 wherein the time required for said control signal to propagate between the first and second
19 devices is proportional to a length traveled between the two devices comprising the length of the
20 first and second signal paths.

1 27. A computer system, comprising:
2 a microprocessor coupled to a primary bridge device;
3 a main memory array coupled to a memory controller by way of a memory bus, said
4 memory controller integral with said primary bridge device;
5 a secondary bridge device coupled to said primary bridge device by way of a primary
6 expansion bus;
7 an input/output controller coupled to said secondary bridge device by way of a secondary
8 expansion bus;
9 a keyboard coupled to said input/output controller;
10 an adjustable signal delay circuit coupled between a control signal source and a control
11 signal destination, said adjustable signal delay circuit time delays a control signal, said adjustable
12 time delay circuit comprising:
13 a first plurality of signal paths each having two ends, a source end of a selected path
14 of the first plurality of signal paths coupled to the control signal source;
15 a second plurality of signal paths each having two ends, a destination end of a
16 selected path of the second plurality of signal paths coupled to the control signal destination;
17 a spanning circuit coupling the selected path of the first plurality of signal paths to
18 the selected path of the second plurality of signal paths; and

19 wherein the length of a control signal path through the adjustable time delay circuit is at
20 least a the sum of a length of the selected path of the first plurality of signal paths and a length the
21 selected path of the second plurality of signal paths.

1 28. The computer system as defined in claim 27 wherein the spanning circuit further
2 comprises:

3 a medial solder pad;
4 a first zero ohm resistor connecting a remaining end of the selected path of the first
5 plurality of signal paths to the medial solder pad; and
6 a second zero ohm resistor connecting a remaining end of the selected path of the second
7 plurality of signal paths to the medial solder pad.

1 29. The computer system as defined in claim 28 wherein the coupling between the control
2 signal source and the source end of selected path of the first plurality of signal paths further
3 comprises:

4 a source solder pad coupled to said control signal source;
5 a zero ohm resistor connecting the source solder pad to the source end of the selected path
6 of the first plurality of signal paths.

1 30. The computer system as defined in claim 28 wherein the coupling between the control
2 signal destination and the selected path of the second plurality of signal paths further comprises:
3 a destination solder pad coupled to said control signal destination;

4 a zero ohm resistor connecting the destination solder pad to the destination end of the
5 selected path of the second plurality of signal paths.

1 31. The computer system as defined in claim 27 further comprising:
2 the control signal source is a clock source;
3 the control signal destination is the memory controller;
4 the control signal path is a clock signal path; and
5 wherein the memory controller uses a clock signal propagating on the clock signal path as a
6 read clock for reading data from the memory bus.

1 32. The computer system as defined in claim 27 further comprising:
2 the control signal source is a feedback output of a phased locked loop (PLL);
3 the control signal destination is a feedback input of the PLL; and
4 the control signal path is a feedback path of the PLL, and the length of the feedback path
5 controls a phase relationship between an input signal to the PLL and an output signal of the PLL.